Faculty of Computers and Artificial Intelligence

CS221: Logic Design



Assignment no 09: Chapter 08

Note: You can check the exercises after the book Chapter. In our assignment, we are using the 11th edition of "Digital Fundamentals" By Thomas L. Floyd"

- **1. What** is a register?
- **2. What** is the storage capacity of a register that can retain one byte of data?
- **3. What** does the "shift capacity" of a register mean?
- 5. For the data input and clock in Figure 8–47, determine the states of each flip-flop in the shift register of Figure 8–3 and show the Q waveforms. Assume that the register contains all 1s initially.

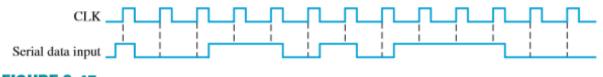
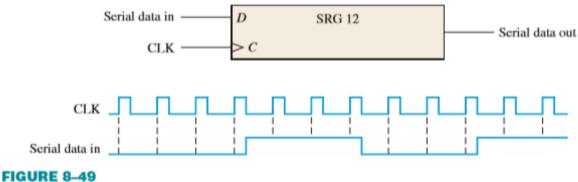


FIGURE 8-47

7. What is the state of the register in Figure 8–49 after each clock pulse if it starts in the 101001111000 state?



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10. A leading-edge clocked serial in/serial out shift register has a data-output waveform as shown in Figure 8–52. **What** binary number is stored in the 8-bit register if the first data bit out (leftmost) is the LSB?

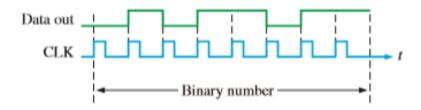
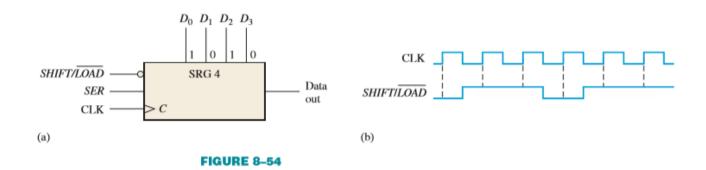
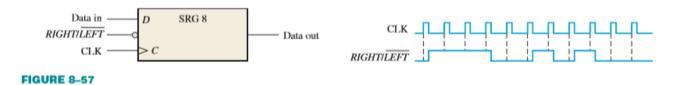


FIGURE 8-52

14. The shift register in Figure 8-54(a) has SHIFT/LOAD and CLK inputs as shown in part (b). The serial data input (SER) is a 0. The parallel data inputs are D0 = 1, D1 = 0, D2 = 1, and D3 = 0 as shown. **Develop** the data-output waveform in relation to the inputs.



21. For the 8-bit bidirectional register in Figure 8–57, **Determine** the state of the register after each clock pulse for the RIGHT/LEFT control waveform given. A HIGH on this input enables a shift to the right, and a LOW enables a shift to the left. **Assume** that the register is initially storing the decimal number seventy-six in binary, with the right-most position being the LSB. There is a LOW on the data-input line.



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27. For the ring counter in Figure 8–60, **Show** the waveforms for each flip-flop output with respect to the clock. **Assume** that FF0 is initially SET and that the rest are RESET. **Show** at least ten clock pulses.

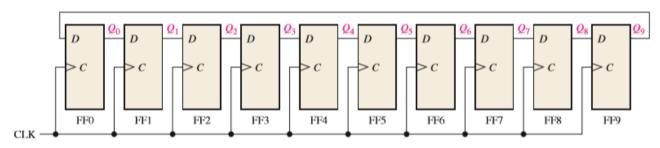


FIGURE 8-60